REMARKS

Favorable reconsideration of the present application is respectfully requested.

The specification is amended to make a minor typographical correction.

Claim 2 has been amended as suggested by the examiner.

Claims 1-8 and 21-28 are present in this application, claims 9-20 are canceled and claims 21-28 are added by way of the present amendment. Claims 7-8 have been withdrawn from consideration. Claims 1 and 6 are amended only to make minor grammatical changes, which do not change the scope of the claim.

Claims 1-5 stand rejected under U.S.C. §102(e) over U.S. 6,281,050 (Sakagami), and claim 6 stands rejected under 35 U.S.C. §103(a) over Sakagami in view of U.S. 6,342,715 (Shimizu et al.).

In the device as recited in claim 1, the bottom layer of the gate electrodes in the cell array region and the bottom layer of the gate electrodes of transistors in the peripheral circuit region are formed before the device isolation insulation is buried, and these bottom layers are maintained in self-alignment with the device isolation insulating film. Such a structure is shown, as a non-limiting example, in Fig. 14. Such a structure avoids the problems associated with a gate electrode formed after the formation of the isolation films, which is illustrated in Figs. 36(a)-(b). Here, retraction occurs along the upper edge of the isolation film 5 due to etching oxide films and then re-growing gate oxide films. The retraction can lead to short-channel effects as well as an increase in leakage current of the peripheral circuit transistors.

Turning to the rejection of claim 1, the bottom layer of the floating gates of the non-volatile memory cells and at least the bottom layer of the gate electrodes of transistors in the peripheral circuit are formed before the device isolation film is buried, and then bottom layer

of the floating gates and the bottom layer of the gate lectrodes of the transistors in the peripheral circuit are maintained in self-alignment with the device isolation insulating film. The Office Action states that the feature of the bottom layers of the transistors being formed before the device isolation insulating film is buried is a "process limitation" and does not contain any weight in a claim drawn to a structure. However, such a device has a different structure from one where the bottom layers of the gate electrodes are not formed before the device isolation insulating film is buried. This is shown, as one example, in Figs. 35(a)-(b) of the present application, and is also shown in Fig. 32 of Sakagami.

In the peripheral transistor forming region of Sakagami, gate oxides 246 and 250 and the fourth poly silicon 252 is formed after the device isolation is formed in apertures 230. Retraction has occurred due to the oxide etching and regrowing of gate oxides (Figs. 27-29), and such a structure is more liable to experience short channel effects and increased leakage current. The circuit with bottom layers formed before the device isolation insulating film as recited in claim 1 has a structure which is different than, and not suggested by, the structure show in Fig. 32 of Sakagami. Accordingly, the structure of claim 1 is patentably distinguishable over Sakagami and withdrawal of this rejection is respectfully requested.

Regarding claim 6, the Office Action correctly found Sakagami not to disclose the peripheral transistor having the three-layer structure recited in claim 6. Shimizu et al, does not teach a three layer structure for the peripheral transistor PT (shown in Fig. 13A), contrary to that stated in the Office Action. The gate of the transistor consists of films 35L and 35U. See column 18, lines 47-59 of Shimizu et al., where gate 35 is made of a two layer conductive material constituted by lower section 35L and upper layer section 35U. Film 37 is the word line which is allowed to extend over the gate, but is electrically insulated from the

gate by film 6. The paragraph beginning at line 66 of column 18 describes how material 37 is allowed to remain over the upper layer section 35U. Film 37 does not constitute a part of the control gate of the transistor PT. As Shimizu et al. does not disclose or suggest the memory device recited in claim 6, withdrawal of the rejection of claim 6 is respectfully requested.

It is also noted that Sakagami is assigned to Kabushiki Kaisha Toshiba (Toshiba Corporation), the assignee of the present application. As Sakagami is available as prior art only under 35 U.S.C. §102(e), it cannot preclude patentability under §103(c). Accordingly, withdrawal of the §103 rejection of claim 6 is respectfully requested.

As the rejection of claim 6 cannot stand since the prior art does not suggest the circuit of claim 6 and Sakagami is not prior art under §103, the final rejection must be withdrawn. Entry of the present amendment is proper and is therefore respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,
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